communications units 22-25 each including a respective transmitter 26-29 and receiver 30-33, with each transmitter 26-29 and each receiver 30-33 all being connected to all three channels A, B, C of a triple-redundant communication link 36. Column 3, lines 46-56.

As taught by Games, each and every receiver 30-33 transmits identical words on all three channels A, B, C at adjacent word periods. Column 3, line 60-column 4, line 10.

The present invention, as recited in claim 1, is a network topology backplane bus architecture wherein one processing node is connected for both transmitting and receiving on a first subset of data communication lines, but is connected for only receiving on a second subset of the data communication lines. A second processing node is connected for both transmitting and receiving on the second subset of said data lines, but is connected for only receiving on the first subset of data lines.

The present invention, as recited in claim 1, is not anticipated by Games because Games fails to teach limiting a first processing node to being connected for only receiving on a second subset of the data communication lines, as recited in claim 1.

Games also fails to teach limiting a second processing node to being connected for only receiving on a first subset of the data communication lines, as is also recited in claim 1.

The Office Action mistakenly suggests that Games teaches one processing node transmitting and receiving on a first subset of data communication lines and receiving on a second subset of data communication lines; and another processing node transmitting and receiving on the second subset of data lines and receiving on the first subset of data lines. The Office Action is wrong.

Rather, Games only teaches having all of the communications units 22-25 being connected for both transmitting and receiving on all three channels A, B, C of triple-redundant communication link 36. Column 3, lines 46-56.

In distinct contrast to Games, the present invention recites having one processing node being coupled for only receiving on less than all, *i.e.*, a first "subset," of the communication lines; while a second processing node is coupled for only receiving on a second subset of the communication lines.

For each of the above reasons, claim 1 is allowable over the Games reference.

Claims 16, 30 and 34 are different in scope from claim 1. However, the above arguments directed to claim 1 are sufficiently applicable to claims 16, 30 and 34 as to make repetition unnecessary. Thus, for each of the reasons above, claims 16, 30 and 34 are believed to be allowable over the Games reference.

Claims 16 and 34 are further distinguished from Games by providing for each of the processing nodes being connected for monitoring data communications transmitted on the subset of communication lines on which they have only receiving privileges, and by receiving data communications on that subset of communication lines only as a function of that monitoring of data communications.

In contrast to the present invention, Games fails to anticipate such monitoring of only a subset of the communication lines because Games teaches a triple-redundant system wherein all of the communications units 22-25 receive identical words on all three channels A, B, C at adjacent word periods. Column 3, line 60-column 4, line 10. Therefore, Games does not even consider the possibility of limiting monitoring and receiving to only a subset of the communications lines, as originally recited in claims 16 and 34.

For each of these additional reasons, claims 16 and 34 are further allowable over the Games reference.

Claim 30 is further distinguished from Games by limiting the first and second processing nodes to receive-only privileges on different first and second subsets of the communication lines.

In contrast to the present invention, Games fails to anticipate dividing the communication lines into mutually exclusive first and second subsets of data communication lines, and limiting the first and second processing node to only receiving privileges on a different ones of the two subsets of communication lines.

For each of these additional reasons, claim 30 is further allowable over the Games reference.

Furthermore, claims 1, 16, 30 and 34 are believed to allowable as originally recited in the patent application as filed. The amendments to claims 1, 16, 30 and 34 are made only to further clarify the subject matter that the Applicants regard as their invention. The

amendments are not believed to be necessary to overcome the cited reference and are not intended to limit the scope of the claims.

Claim Rejections Under 35 USC § 103

Claims 2-15, 17-29 and 31-33 were rejected under 35 USC § 103(a) as being obvious over Games in view of US Patent 5,325,517 to Baker et al.

Claims 2-15, 17-29 and 31-33 depend from base claims 1, 16 and 30, respectively.

The invention recited in claim 1 is patentable over Games and Baker, both individually and in combination. As discussed above, Games teaches in relevant part a multi-redundant data synchronized transmission system in which multiple communications units 22-25 each have a transmitter 26-29 and a receiver 30-33 all being connected to all three channels A, B, C of a triple-redundant communication link 36. Column 3, lines 46-56. Each and every receiver 30-33 transmits identical words on all three channels A, B, C at adjacent word periods. Column 3, line 60-column 4, line 10.

As is also discussed above, Games fails to provide the communication lines being divided into first and second subsets, and the different processing nodes being coupled to transmit and receive on a first subset of communication lines, while being restricted from transmitting on a second subset by being limited to only receiving on that second subset of communication lines.

Baker teaches a fault tolerant data processing system wherein a first plurality of processing units concurrently perform identical operations under program control, each processor unit being coupled to hardware including fault tolerant I/O devices and storage, in which fault tolerant operations are continued so long as two of the units whose states can be compared are error free. See, Abstract.

The Baker reference fails to provide the deficiencies of Games. Baker fails to disclose or suggest either a first processing node connected for only receiving on one subset of data communication lines, or a second processing node connected for only receiving on a different subset of data communication lines, as presently recited in claim 1.

Rather, as the Office Action notes, Baker merely provides that a plurality of processing nodes may be interconnected via a network in a fault-tolerant environment.

For each of the above reasons, base claim 1 is believed to be allowable over the Games and Baker references, both individually and in combination. Claims 2-15 are allowable at least as depending from allowable base claim 1.

Base claims 16 and 30 are different in scope from claim 1. However, the above arguments directed to claim 1 are sufficiently applicable to claims 16 and 30 as to make repetition unnecessary. Thus, for each of the reasons above, claims 16 and 30 are believed to be allowable over the Games and Baker references.

Base claims 16 and 30 are additionally allowable as reciting monitoring of the subset of communication lines and receiving transmissions on the monitored communication lines as a function of the monitoring.

Claims 17-29 and 31-33 are allowable at least as depending from allowable base claims 16 and 30, respectively.

Regarding claims 5-7 the Office Action suggests that Games, at column 5, line 24-column 6, line 67, discloses utilizing the first subset of data communication lines for communicating with another of the processing nodes. The Office Action is wrong.

Rather than disclosing or suggesting utilizing the first subset of data communication lines for communicating with another of the processing nodes, as recited in claims 5-7, Games teaches, at column 5, line 24-column 6, line 67, Games merely teaches that if one of the receivers 30-33 fails o recognize its unit designation that it will ignore the data being transmitted. Thus, in stark contrast to the present invention, Games teaches limiting the communications units 22-25 ability to receive data on one or more of the channels A, B, C of triple-redundant communication link 36. Column 5, lines 31-41. The present invention rather limits the processing nodes ability to transmit data on a subset of the communication lines by the processing node being connected for only receiving on the second subset of data communication lines, as recited in claim 1.

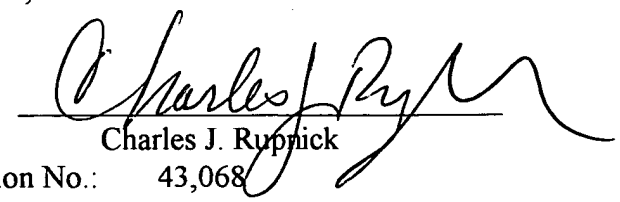
For each of the above reasons, claims 5-7 are allowable over the Games reference independently of base claim 1.

The claims now being in form for allowance, reconsideration and allowance is respectfully requested.

For the Examiner's convenience, a clean copy of the claims, including the changes thereto, are provided in an Attachment hereto.

If the Examiner has questions or wishes to discuss any aspect of the case, the Examiner is encouraged to contact the undersigned at the telephone number given below.

Respectfully submitted,

Attorney: 
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Attachment Showing Claims With Amended Matter Incorporated

IN THE CLAIMS

1. (Amended) A network topology backplane bus architecture comprising:

a plurality of independent data communication lines;

a plurality of processing nodes sharing said independent data communication lines for data communication;

one of said processing nodes being connected for both transmitting and receiving on a first subset of said data communication lines and being connected for only receiving on a second subset of said data communication lines; and

another of said processing nodes being connected for both transmitting and receiving on said second subset of said data lines and being connected for only receiving on said first subset of said data lines.

2. The network topology backplane bus architecture recited in claim 1, wherein ones of said independent data communication lines comprise a first independent data communication network and different ones of said independent data communication lines comprise a second independent data communication network.

3. The network topology backplane bus architecture recited in claim 2, wherein ones of said first subset of said data communication lines in combination with ones of said second subset of said data communication lines comprise one of said first and second independent data communication networks; and

different ones of said first subset of said data communication lines in combination with different ones of said second subset of said data communication lines comprise a different one of said first and second independent data communication networks

4. The network topology backplane bus architecture recited in claim 1, wherein said one of said processing nodes transmitting and receiving on a first subset of said data

communication lines utilizes said first subset of said data communication lines for local communication within said processing node.

5. The network topology backplane bus architecture recited in claim 4, wherein said one of said processing nodes transmitting and receiving on a first subset of said data communication lines further utilizes said first subset of said data communication lines for broadcasting transmissions to another of said processing nodes.

6. The network topology backplane bus architecture recited in claim 4, wherein said one of said processing nodes transmitting and receiving on a first subset of said data communication lines further utilizes said first subset of said data communication lines for receiving data transmissions from another of said processing nodes.

7. The network topology backplane bus architecture recited in claim 4, wherein said one of said processing nodes transmitting and receiving on a first subset of said data communication lines is one of a plurality of said processing nodes transmitting and receiving on said first subset of said data communication lines.

8. The network topology backplane bus architecture recited in claim 7, wherein each of plurality of processing nodes transmitting and receiving on said first subset of said data communication lines are co-located in a first resource enclosure.

9. The network topology backplane bus architecture recited in claim 7, wherein each of plurality of processing nodes transmitting and receiving on said first subset of said data communication lines time-shares said data communication lines with others of said plurality of processing nodes transmitting and receiving on said first subset of said data communication lines.

10. The network topology backplane bus architecture recited in claim 9, wherein each of plurality of processing nodes transmitting and receiving on said first subset of said data communication lines time-shares said data communication lines in synchronization with others of said plurality of processing nodes transmitting and receiving on said first subset of said data communication lines.

11. The network topology backplane bus architecture recited in claim 5, wherein said processing node transmitting and receiving on said second subset of said data lines and receiving on said first subset of said data lines utilizes said second subset of said data communication lines for local communication within said processing node.

12. The network topology backplane bus architecture recited in claim 11, wherein said processing node transmitting and receiving on said second subset of said data communication lines further utilizes said second subset of said data communication lines for broadcasting transmissions to another of said processing nodes.

13. The network topology backplane bus architecture recited in claim 12, wherein ones of said processing nodes supports different ones of flight critical functions.

14. The network topology backplane bus architecture recited in claim 13, wherein one or more of said processing nodes supporting one of said flight critical functions is duplicated in one or more additional ones of said processing nodes.

15. The network topology backplane bus architecture recited in claim 14, wherein one of said processing nodes supporting said one of said flight critical functions is located in a first resource enclosure; and

at least one of said additional processing nodes supporting said one of said flight critical functions is located in a physically isolated second resource enclosure.

16. (Amended) A network topology backplane bus architecture comprising:

a plurality of processing nodes transmitting and receiving data communications;

a plurality of independent data communication networks formed of a plurality of independent data communication lines, a subset of said data communication networks extending between ones of said plurality of processing nodes;

a first subset of ones of said data communication lines allocated to a first of said processing nodes for transmitting and receiving data communications, said first subset of said data communication lines further allocated to a second of said processing nodes for monitoring data communications transmitted on said first subset of said data communication lines and receiving data communications as a function of said monitoring of said data communications transmitted on said first subset of said data communication lines;

a second subset of ones of said data communication lines allocated to said second processing nodes for transmitting and receiving data communications, said second subset of said data communication lines further allocated to said first processing nodes for monitoring data communications transmitted on said second subset of said data communication lines and receiving data communications as a function of said monitoring of said data communications transmitted on said second subset of said data communication lines.

17. The network topology backplane bus architecture recited in claim 16, wherein each of said plurality of processing nodes supports one or more processing functions.

18. The network topology backplane bus architecture recited in claim 17, wherein said first subset of said data communication lines comprises ones of said plurality of independent data communication lines forming each two or more of said plurality of independent data communication networks; and

said second subset of said data communication lines comprises different ones of said plurality of independent data communication lines forming each two or more of said plurality of independent data communication networks.

19. The network topology backplane bus architecture recited in claim 17, wherein said subset of said data communication networks extending between ones of said plurality of processing nodes comprises:

said first subset of ones of said data communication lines allocated to said first processing node for transmitting and receiving data communications; and

said second subset of ones of said data communication lines allocated to said second processing node for transmitting and receiving data communications.

20. The network topology backplane bus architecture recited in claim 19, wherein said first processing node is one of a plurality of first processing nodes each transmitting and receiving on said first subset of data communication lines; and

said second processing node is one of a plurality of second processing nodes each transmitting and receiving on said second subset of data communication lines.

21. The network topology backplane bus architecture recited in claim 20, wherein each of said plurality of first processing nodes are co-located in a first resource enclosure.

22. The network topology backplane bus architecture recited in claim 20, wherein each of said plurality of first processing nodes time-shares said data communication lines with others of said plurality of first processing nodes.

23. The network topology backplane bus architecture recited in claim 20, wherein one or more of said processing nodes supporting one of said processing functions is duplicated in one or more additional ones of said processing nodes.

24. The network topology backplane bus architecture recited in claim 23, wherein a first one of said processing nodes supporting said one of said processing functions is located in a first resource enclosure; and

at least one of said additional processing nodes supporting said one of said processing functions is physically isolated from said first one of said processing nodes in a second resource enclosure.

25. The network topology backplane bus architecture recited in claim 17, wherein said first subset of data communication lines allocated to a first of said processing nodes for transmitting and receiving data communications and said second subset of data communication lines allocated to said second processing node for transmitting and receiving data communications comprises a first of said data communication networks, said first data communication networks extending between ones of said plurality of processing nodes;

additional different ones of said plurality of independent data communication lines comprise a second of said data communication networks allocated to said first processing nodes for transmitting and receiving data communications among said first processing nodes; and

additional different ones of said plurality of independent data communication lines comprise a second of said data communication networks allocated to said second processing nodes for transmitting and receiving data communications among said second processing nodes.

26. The network topology backplane bus architecture recited in claim 25, wherein said first processing nodes comprise a single processing node supporting a first processing function; and

said second processing nodes comprise a single processing node supporting a second processing function.

27. The network topology backplane bus architecture recited in claim 26, wherein said first and second processing nodes are co-located in a single resource enclosure.

28. The network topology backplane bus architecture recited in claim 26, wherein said first and second processing nodes are located in respective first and second physically isolated resource enclosures.

29. The network topology backplane bus architecture recited in claim 26, wherein said first processing function and said second processing functions are essentially identical processing functions.

30. (Amended) A method of sharing independent data communication lines for fault tolerant data communication among a plurality of processing nodes, the method comprising:

dividing a plurality of data communication lines into mutually exclusive first and second subsets of data communication lines;

permitting first processing nodes both transmitting and receiving privileges on said first subset of data communication lines and limiting second processing nodes to only receiving privileges on said first subset of data communication lines;

permitting to the second processing nodes both transmitting and receiving privileges on said second subset of data communication lines and limiting the first processing nodes to only receiving privileges on said second subset of data communication lines.

31. The method recited in claim 30, further comprising extending said first and second subsets of data communication lines between the first and second processing nodes.

32. The method recited in claim 31, further comprising isolating ones of said first subset of data communication lines and ones of said second subset of data communication lines from other different ones of said first and second subsets of data communication lines.

33. The method recited in claim 30, wherein said first and second subsets of data communication lines comprise a single subset of inter-nodal data communication lines;

and further comprising:

permitting both the first and second processing nodes to both transmit and receive on said inter-nodal data communication lines;

permitting the first processing nodes to both transmit and receive on a first additional subset of data communication lines; and

permitting the second processing nodes to both transmit and receive on a second additional subset of data communication lines.

34. (Amended) A method of sharing independent data communication lines for fault tolerant data communication among a plurality of processing nodes, the method comprising:

permitting first processing nodes to both transmit and receive on a first subset of data communication lines and limiting the first processing nodes to only monitor transmissions on a second subset of data communication lines and to receive transmissions as a function of detecting transmissions on said second subset of data communication lines;

permitting second processing nodes to both transmit and receive on said second subset of data communication lines and limiting the second processing nodes to only monitor transmissions on said first subset of data communication lines and to receive transmissions as a function of detecting transmissions on said first subset of data communication lines.